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10ES33

Third Semester B.E. Degree Examination, June/July 2018
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Reduce the following function using K-Map technique and implement using gates :
$J = f(A, B, C, D, E) = \Sigma_m (4, 5, 6, 7, 9, 11, 13, 15, 25, 27, 29, 31)$
$G = f(A, B, C, D) = \pi M(0, 4, 5, 7, 8, 9, 11, 12, 13, 15)$. **(12 Marks)**

b. Fig.Q1(b) shows a BCD counter that produces a 4-bit output representing the BCD code for the number of pulses that have been applied to the counter input. The counter resets to "0000" on the tenth pulse and starts recounting. Design the logic circuit that produces a "High" output whenever the count is 2, 3, or 9. Use K–Mapping and implement the logic circuit using NAND gates. **(08 Marks)**

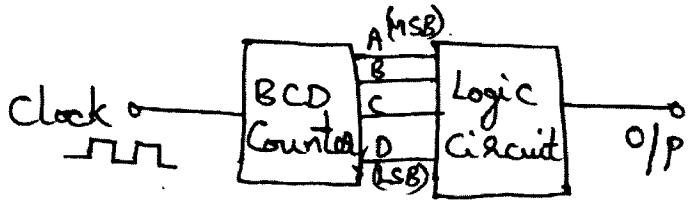

Fig.Q1(b)

2 a. Convert the given Boolean function $f(x, y, z) = [x + \bar{x}\bar{z}(y + \bar{z})]$ into maxterm canonical form and hence highlight the importance of canonical formula. **(06 Marks)**

b. Simplify using Quine Mc Cluskey tabulation algorithm.
$v = f(a, b, c, d) = \Sigma(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$. **(14 Marks)**

3 a. Implement a full subtractor using decoder and write the truth table. **(10 Marks)**

b. What are the problems associated with the basic encoder? Explain how they can be overcone by priority encoder, considering 8 input lines. **(10 Marks)**

4 a. Design a combinational circuit that accepts two unsigned, 2-bit binary number $A = A_1 A_0$ and $B = B_1 B_0$ and provide 3 outputs corresponding to A = B, A > B and A < B. **(08 Marks)**

b. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 9, 10, 15)$ using :
i) 8 : 1 MUX with a, b, c as select line
ii) 4 : 1 MUX with a, b as select lines. **(08 Marks)**

c. Explain the terms :
i) Ripple–carry propagation
ii) Look–ahead carry. **(04 Marks)**

PART – B

5 a. What is a flip-flop? Discuss the working principle of S-R flip-flop with its truth table. Also explain the role of S-R latch in switch debouncer circuit. **(08 Marks)**

b. With neat schematic diagram of master slave JK-FF, discuss its operation. Mention the advantages of JK-FF over master slave SR-FF. **(12 Marks)**

6 a. Design a 4-bit universal shift register using positive edge triggered D-flip-flops to operate a shown in table below TableQ6(a). **(12 Marks**

Select line		Data line selected	Register Operation
S_1	S_0		
0	0	I_0	Hold
0	1	I_1	Shift right
1	0	I_2	Shift left
1	1	I_3	Parallel load

Table Q6(a)

b. Explain the working of a 4-bit asynchronous DeCade counter using JKFF in toggel mod **(08 Mark**

7 a. Explain mealy and Moore sequential circuit models. **(04 Mark**

b. For the state machine M_1 shown in Fig.Q7(b) obtain,

i) State table
ii) Transition table
iii) Excitation table for T flip-flop
iv) Logic circuit for T excitation realization. **(16 Mark**

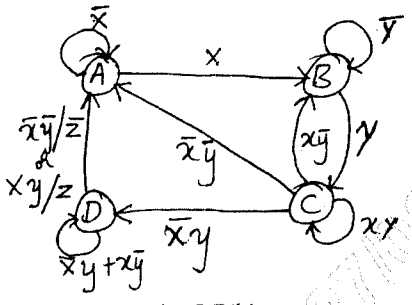

Fig.Q7(b)

8 a. Construct Moore and Mealy state diagram that will detect input sequence 10110, when inp pattern is detected Z is asserted high. Give state algorithms for each state. **(10 Mark**

b. Design a cyclic Mod6, synchronous binary counter using J-K flip-flop. Give the sta diagram, transition table and excitation table. **(10 Mark**

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